

IMPERIAL COLLEGE OF SCIENCE TECHNOLOGY AND MEDICINE
UNIVERSITY OF LONDON

DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING
M.Eng. and A.C.G.I. EXAMINATIONS 2008

PART IV

INTRODUCTION TO DIGITAL IC DESIGN

SOLUTIONS

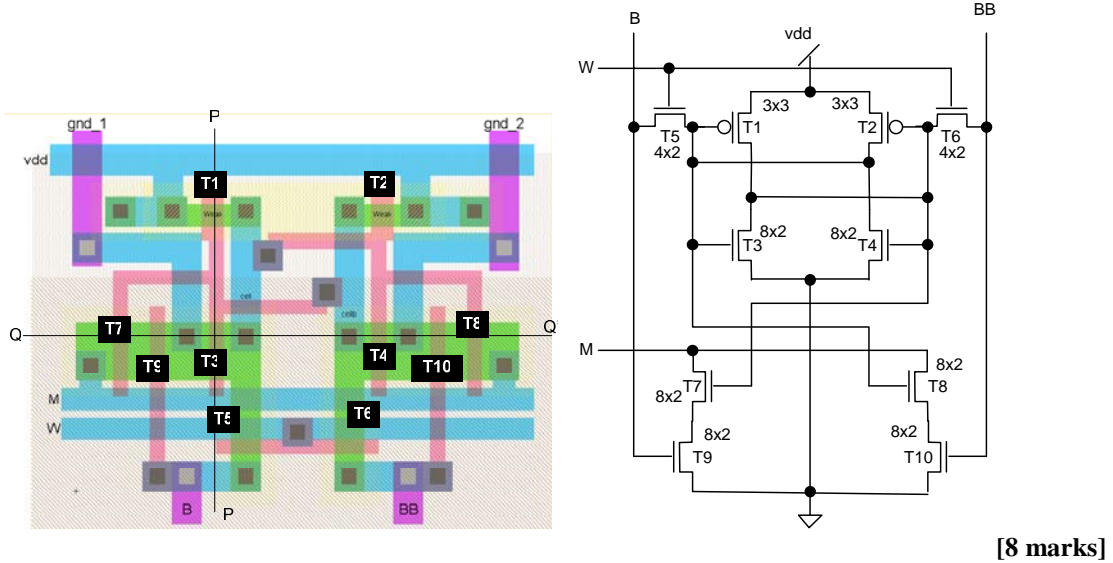
This is an open-book examination.

You may need red, green, blue, yellow and black coloured pens.

First Marker: *Peter Cheung*
Second Marker: *Christos Bouganis*

Solution to Question 1

- a) This question tests student's ability to understand a full custom layout. The extracted circuit with transistor sizes should be:



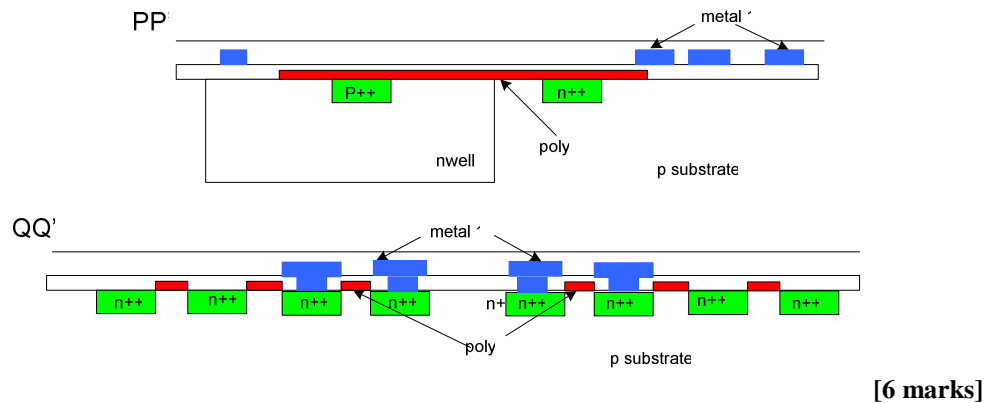
- b) This is a circuit for 1-bit content-addressable memory (CAM). W is the word line signal. When it is enable, a word is written to or read from the one bit memory formed by the crossed coupled inverters. B and BB' are the bit and bit-bar signals. M is the Match signal which is pulled down if the B/BB' values matches those stored in the one-bit memory cell.

[3 marks]

- c) Nwell contacts, which normally connect the n-well region to vdd, and substrate contacts, which connect the substrate to ground, are missing in this layout. As a result this circuit is susceptible to latchup, which is the stray thyristor circuit shorting vdd to ground. To avoid this, just add nwell and substrate contacts everywhere.

[3 marks]

- d) This part of the question tests student's ability to relate the layout to the physical process and different layers on the chip.



Solution to Question 2

a) Each student took part in a group design project in teams of 4 or 5 to design a full-custom chip in the Autumn term. This question provides recognition of individual contribution to, and understanding of, the project.

[9 marks]

b) This part of the question test students appreciation of the advantages and disadvantages of full-custom design as compared to other design styles. The answer would depend on the nature of the chip designed. For example, for the Median Filter chip or the neural network chip, the full-custom design provides much more efficient design due to the tile-like nature of the chip.

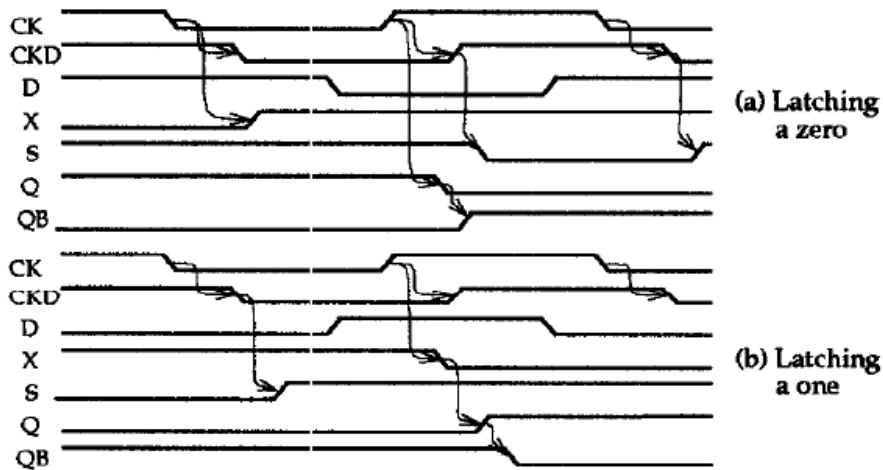
[5 marks]

c) Testing strategy is one of the most important aspects of the designs. However, not all chips designed on this course actually implemented a testing strategy. The second part of this section provide an alternative choice. In particular students are expected to learn from what they have done in the project any suggest improvements.

[6 marks]

Solution to Question 3

- a) This is a semidynamic D flip-flop as proposed by Klass (ISVLSI 1998, "Semi-Dynamic and Dynamic Flip-flops with Embedded logic"). Similar to the pulsed latch, this operates on the principles of intersecting pulses. While the clock is low, X precharges high and Q holds its old value. When the clock rises, the dynamic NAND formed by T3 and T4 evaluates. If D is '0', X remains high and the top nMOS transistor turns OFF. If D is '1', X is pulled own to ground. This allows for a very short pulse and short hold time. The operation of this flip-flop for latching '0' and '1' are demonstrated in the following timing diagrams (from Klass' paper):

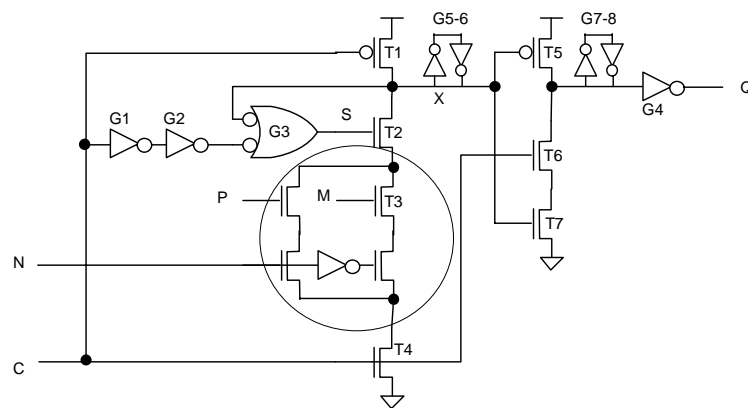


[8 marks]

- b) The inverters G5-8 must be designed to have weak transistors so that they do not fight with the pullup and pulldown transistors. If they are removed, this becomes a purely dynamic circuit, which will not work if the clock stops altogether.

[3 marks]

- c)



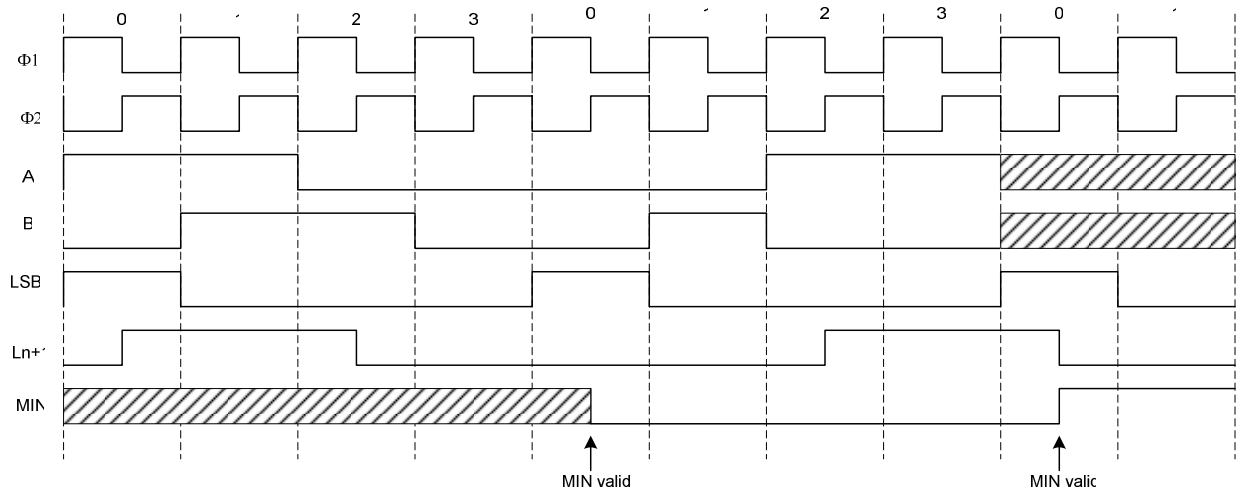
[3 marks]

- d) The layout depends on student's design.

[6 marks]

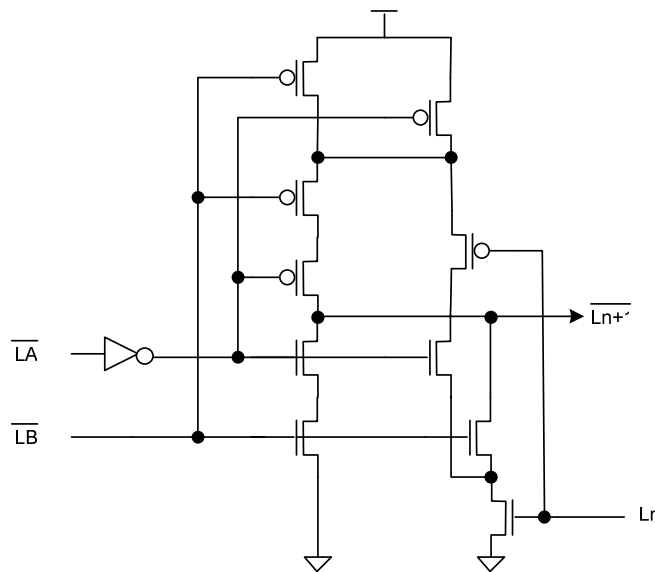
Solution to Question 4

(a) Need to show at least 9 cycles.



[10 marks]

(b)



[10 marks]

Solution to Question 5

This question tests student's ability to apply the Method of Logical Effort (from Ivan Sutherland) to simple circuits and to size transistors.

- a) Both logic effort and electrical effort round the loop of an n-stage ring oscillator are independent of transistor sizes, therefore the delay must also be independent of transistor sizes. The frequency of oscillation allows us to derive the delay of a unit delay inverter. Students are expected to show how this can be done including loading effects of the measurement circuit. Mostly bookwork.
- b) This can be done in more than one way. The easiest is to divide the circuit into three stages as shown in the diagram. Recognize that the critical signal path is through the NAND function of stage 2, the logical and electrical efforts (per input) for the three stages are:

	Logical Effort	Electrical Effort
Stage 1	4/3	1
Stage 2	4/3	3/2
Stage 3	1	10

$$\text{Total delay (ignoring parasitic delay)} \approx \frac{4}{3} + 2 + 5 = 13\frac{1}{3}$$

- c) Assume stage 2 is scaled by X and stage 3 by Y. The best delay is obtained when stage 2 & 3 have equal delay.

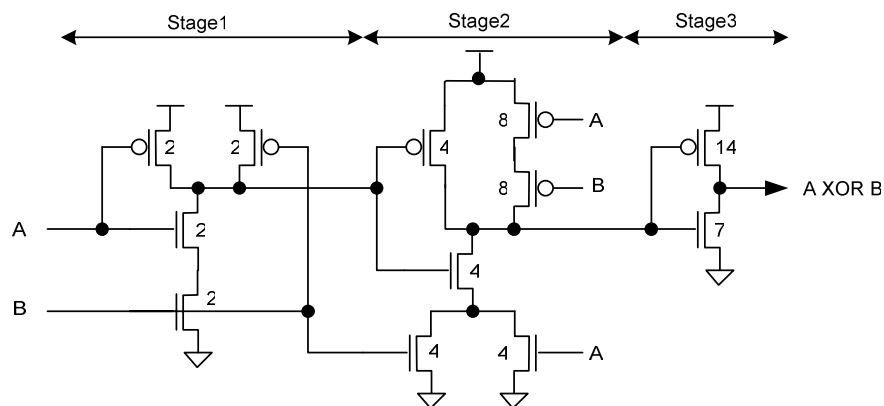
$$\begin{aligned} \text{Delay1} &= D1 = (4/3)X \\ \text{Delay2} &= D2 = 2Y/X \\ \text{Delay3} &= D3 = 10/Y \end{aligned}$$

$$\text{Assuming } 2Y/X = 10/Y \Rightarrow X = (1/5)Y^2$$

$$\text{Total delay } D = D1 + D2 + D3 = (4/3)(1/5)Y^2 + 10/Y + 10/Y = \frac{4}{15}Y^2 + \frac{20}{Y}$$

To get the best delay, we find:

$$\left. \frac{dD}{dY} \right|_{\min} = \frac{8}{15}Y - \frac{20}{Y^2} = 0 \Rightarrow Y^3 = \frac{75}{2} \Rightarrow Y \approx 3.5 \quad \text{and } X \approx 2$$



Total delay $D \approx 9$ unit inverter delays.

Solution to Question 6

This question examines student's understanding in test and design for test.

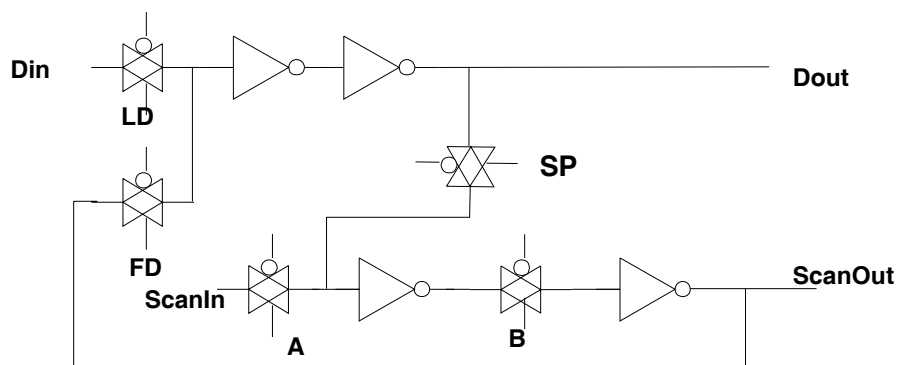
- a) Scan-path registers improve testability of digital circuits by:
- Breaks feedback path in sequential circuits
 - Provides controllability - can force a state onto a sequential circuit
 - Provides observability - can obtain hidden states and hidden nodes
 - Excellent ATPG tools available for designs with full-scan path inserted.

Disadvantages: Can increase test time by a large factor.

Add scan-path at all internal busses. Must be careful with register file due to bi-directional bus.

[8 marks]

b)



How it works:

- 1) To latch data, pulse LD, FD=0, SP=0
- 2) To shift data along scan path, pulse A, then pulse B
- 3) To transfer register data to scan path, pulse SP then pulse B
- 4) To force a data value from scan path to latch, pulse FD.

If SP, FD and B are pulsed, we swap scan path data with those of the register and therefore we sample the response of the circuit while forcing the next test vector.

[6 marks]

c)

From circuit,

$$Z = \overline{\overline{(A + B)} + (D + E + F)}$$

or

$$Z = \overline{ABDEF}$$

Therefore C is totally redundant. Hence node is not testable.

[6 marks]