

Exam 2008 - SOLUTIONS

1/15

Q1/ Bandgap voltage reference circuit has almost zero temperature coefficient. Used mainly as stable voltage reference in ICs.

2

PTAT (Proportional to absolute temperature) current generator. Output current usually insensitive to power supply voltage. Used as a biasing circuit in most precision ICs.

2

For BG reference :- $V_{BE1} = V_{BE2} + I_2 R_3$ (B) (1)

Since $V_{BE1} - V_{BE2} = V_T \ln(I_1/I_2)$

then $V_0 = V_{BE3} + (R_2/R_3) V_T \ln(I_1/I_2)$
 \uparrow
 $V_T \ln(I_1/I_2) \rightarrow$ assume room temp.

for $dV_0/dT = 0$, then $dV_{BE3}/dT = \frac{V_T R_2 \ln(I_1/I_2)}{T R_3}$

Since $\frac{dV_{BE}}{dT} = -2.5 \text{ mV}/^\circ\text{C}$, $\frac{V_T}{T} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}}$

then $(\frac{R_2}{R_3}) \ln(\frac{I_1}{I_2}) = 29$ and so

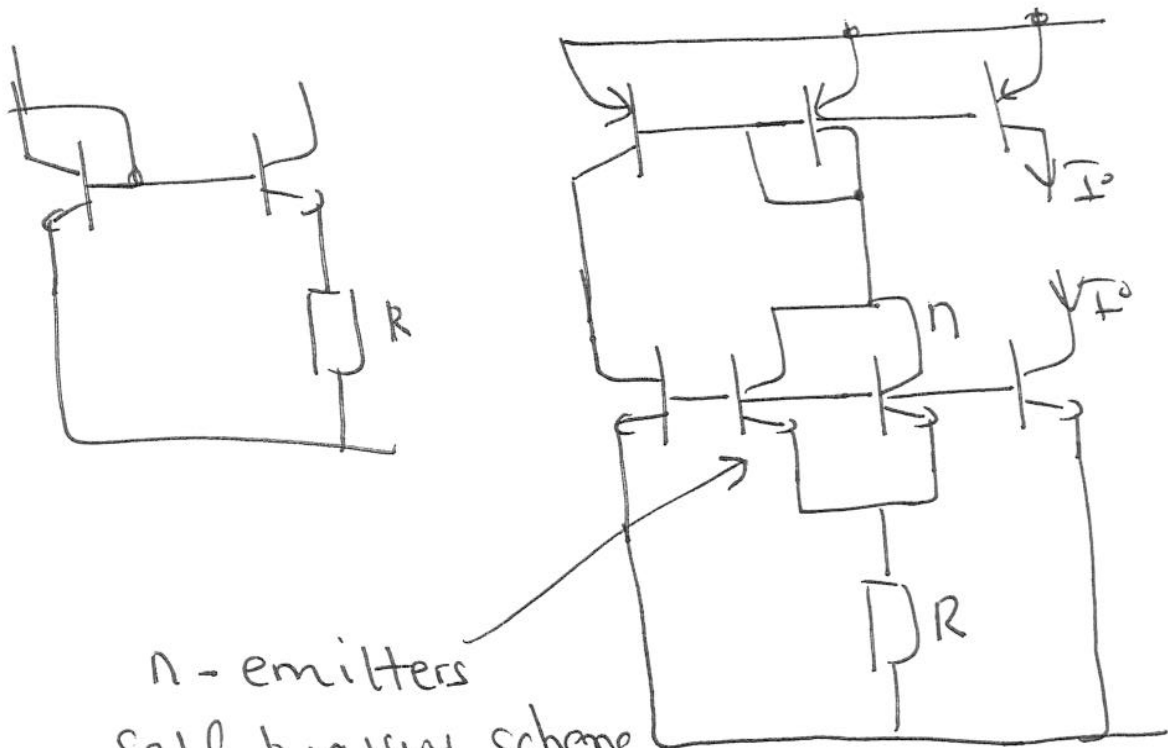
$$V_0 = 1.283 \text{ V}$$

8

CT

Question 1 continued.

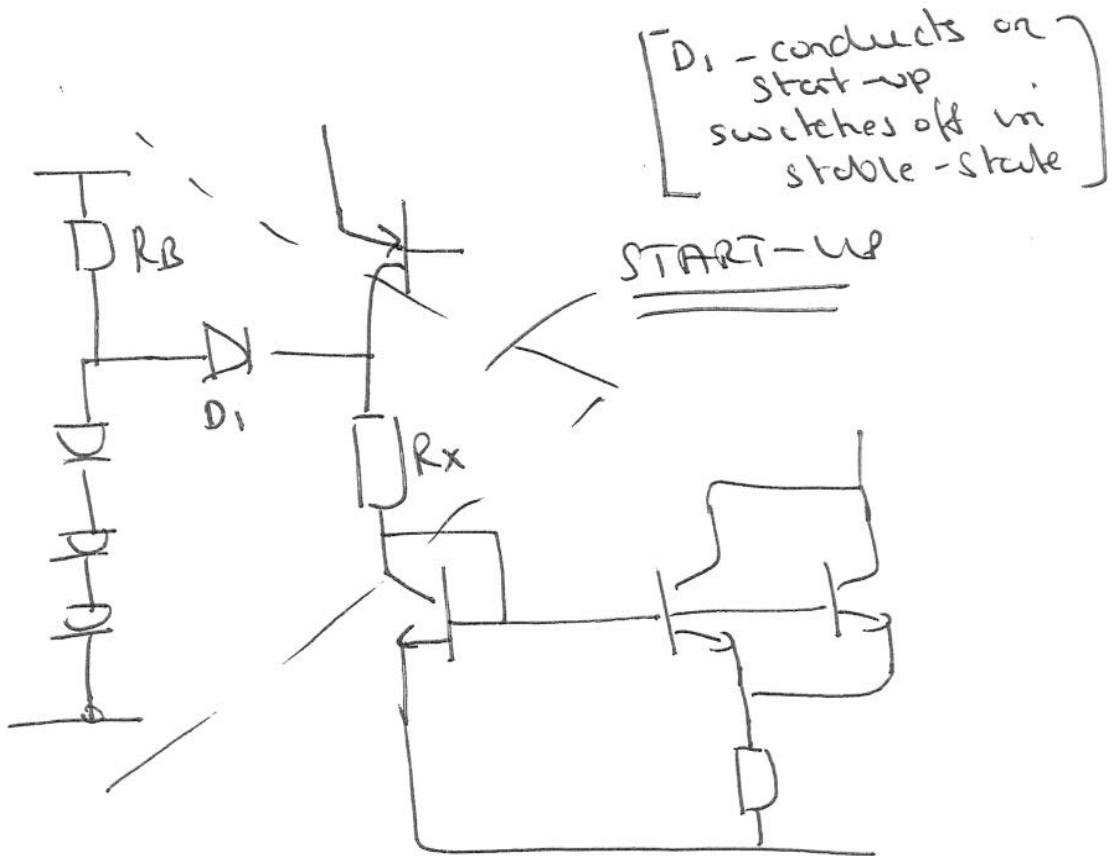
2



n-emitters
self biasing scheme
requires start up.

5

$$I_0 = \frac{V_T}{R} \ln [n]$$



4

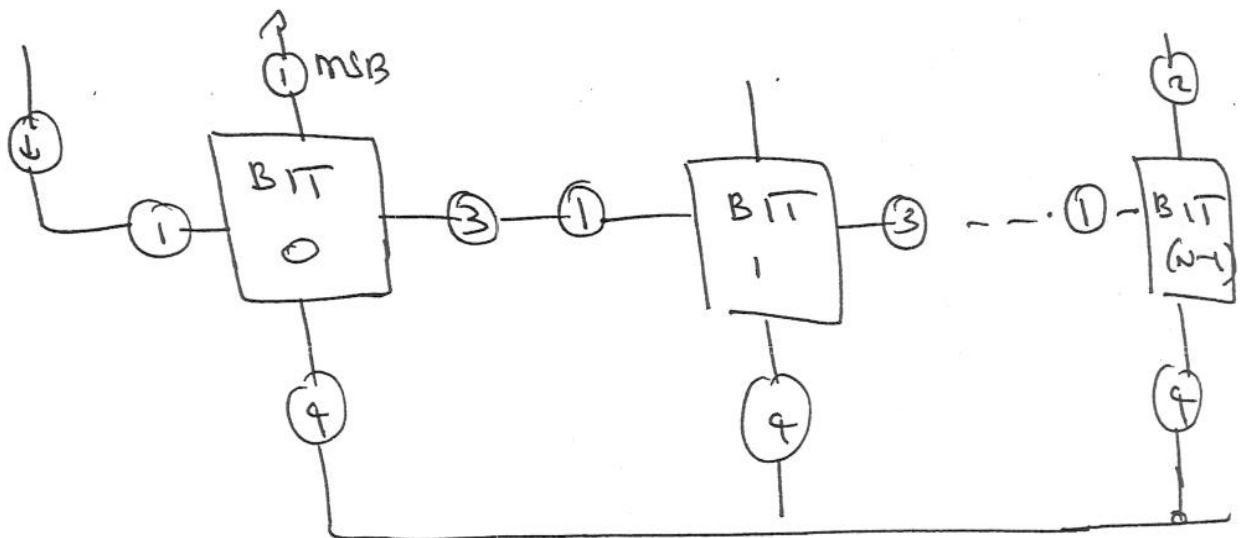
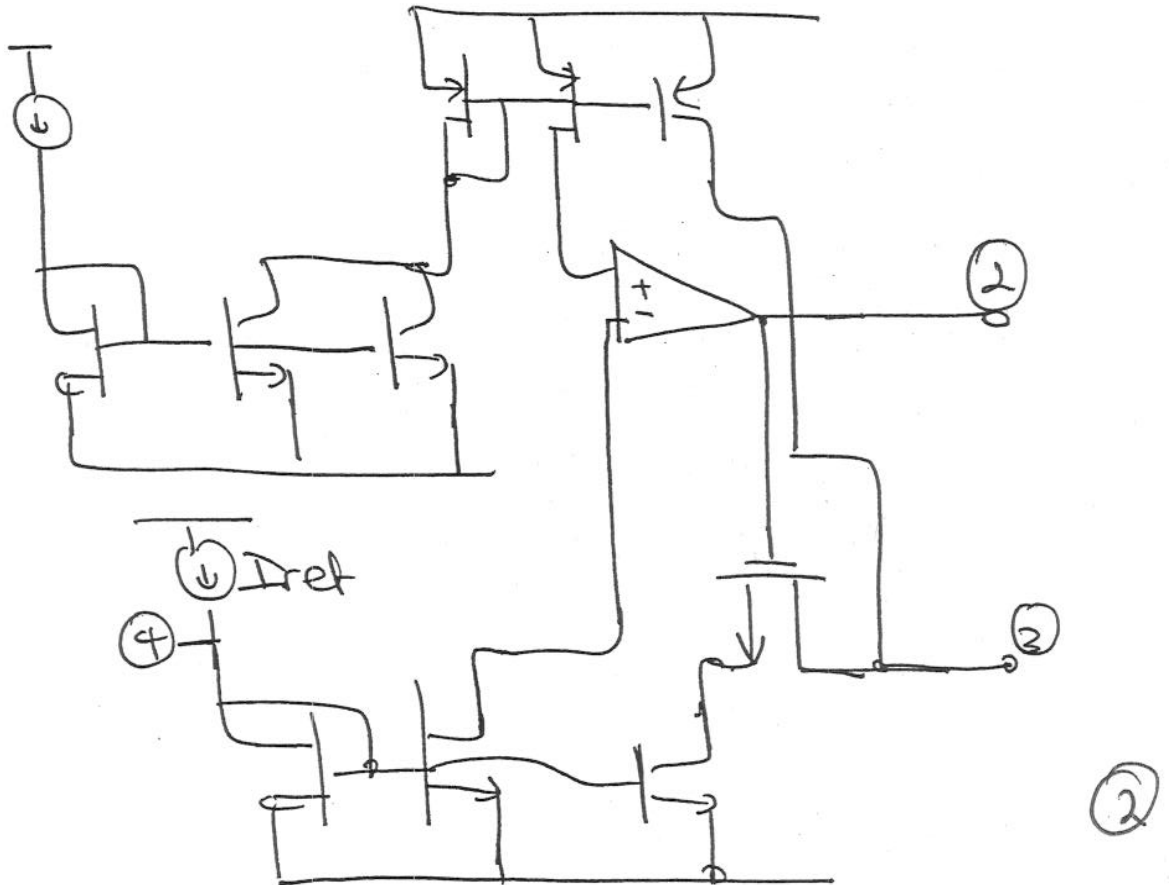
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Question 2

Allgemeine Converter

1 Bit



BASIC ARCHITECTURE

(3)

CT

(2)

if $2I_{in} < I_{ref}$

Comp goes low, digital output = 0
and analogue output $2I_{in}$.

if $2I_{in} > I_{ref}$, comp output goes
high, digital = 1

Analogue output $(2I_{in} - I_{ref})$

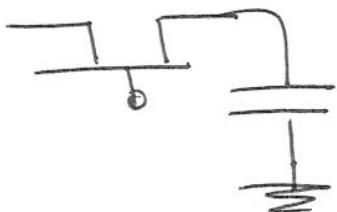
Analogue output feeds into following bit
which performs exactly the same function.
The process is repeated on many times
as necessary to achieve the desired
resolution.

6

~||~

Last part

$$DR \triangleq V_{ref}/noise = 2^N$$



RMS noise of switch
capacitor

$$\sqrt{\frac{kT}{C}}$$

CT

Assume $f_c = \frac{1}{10 \cdot R \cdot C}$, then

Solving for C gives

$$DR = 2^N = V_{eff} / \sqrt{kT \cdot 10 \cdot R \cdot f_c}$$

$$R_{ov} = \frac{1}{2\beta (V_{GS} - V_T)} \approx \frac{1}{(2\beta \times 4)}$$

$$\beta = \left(\frac{\mu W}{2L} \right)$$

Can now find DR @ 40kHz.

(10)

Question 3

(a) Floating integrated RC integrator.

Double mos differential

$$R = \frac{V_{in} - (-V_{in})}{(I_1 - I_2)} = \frac{1}{2\beta(V_{C1} - V_{C2})} \Rightarrow \text{Expected head derivation.}$$

$$T_{\sim} RC = \frac{C}{2\beta(V_{C1} - V_{C2})} \quad \text{--- (A) (B)}$$

(b) Differential, parasitic insensitive SC integrator. During one switch phase C_1 charges to $(V_1 - V_2)$ such that $I_{C1} = 1/T (V_1 - V_2) C$ or $f_c C_1 (V_1 - V_2)$ where $f_c = \text{clock frequency}$.

During the 2nd clock phase

$$I_{C1} = I_{C2} = j\omega C_2 V_0$$

$$\therefore V_0 = \frac{C_1}{C_2} \left[\frac{f_c}{j\omega} \right] (V_1 - V_2)$$

Assumes $f_c \gg 2\pi/\omega$

$$T_{\sim} = \left[\frac{C_2}{C_1 f_c} \right] \rightarrow \text{(A) (B)}$$

(6)

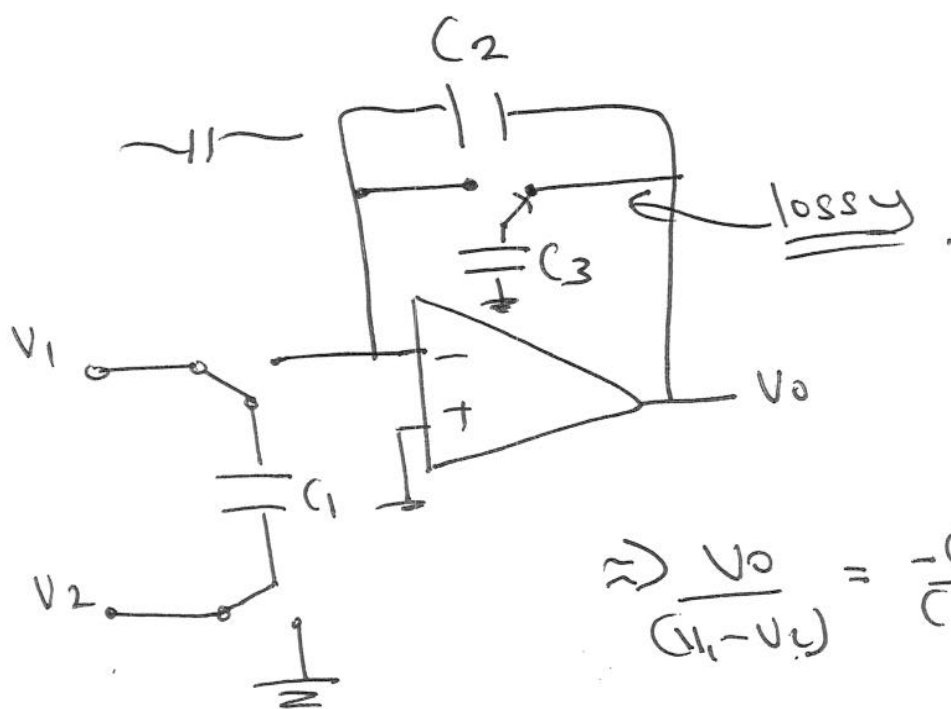
(T)

Question 3 - continued.

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Continuous-time \rightarrow Fast
 \rightarrow potential low power
 \rightarrow inaccurate / need tuning

Switched-cap \rightarrow Accurate
 \rightarrow low frequency
 \rightarrow higher power
 \rightarrow precision (cap ratios)



(4)

$$\approx \frac{V_o}{(V_1 - V_2)} = \frac{-C_1}{C_3} \left[\frac{1}{C_1 + j\omega \frac{C_2 T}{C_3}} \right]$$

(4)

(7)

CT

Q4.

8

a) Bandgap reference. Output voltage reference independent of temperature.

Assumes $V_{BE} \approx -2.5 \text{ mV}/^\circ\text{C}$

Analysis $\beta \gg 1$

$$V_{BE3} - V_{BE2} = V_{TH} (\ln I_1 / I_2) = I_2 R$$

$$\text{Thus } V_0 = V_{BE3} + (R_2/R_3) (V_T) \ln I_1 / I_2$$

For $dV_0/dT = 0$, then $(R_2/R_3) \ln I_1 / I_2 \approx 24.5$, $V_0 = 1.283 \text{ V}$ (2)

b) V_{GS} multiplier. Can replace stacked diodes with a single resistor for biasing purposes.

$$V_0 \approx V_{GS} [1 + R_2/R_1]$$

$$\approx (1 + R_2/R_1) [V_T + \sqrt{I_D/\beta}]$$
 (2)

c) PTAT (proportional to absolute temperature) constant current source/sink. The output current is virtually independent of the power supply voltages. Diode char R_B and R_N form automatic start-up circuitry ensure circuit behaves in correct output state. (4)

Analysis - Assuming matched devices $\beta \gg 1$

then $I_0 = \Delta V_{BE} / R = [V_T \ln(I_{IN}/I_0) (I_{S3}/I_{S1})] / R$
 $(I_{S3} = 2I_{S1})$ then $\underline{I_0 = (V_T \ln 2) R}$ (2)

Question 4 - continued.

Fig 4d \Rightarrow

Regulated cascode current sink,
 since drain-source voltage of Q_1 is
 regulated by the feedback amplifier
 Q_2 the current has a very high
 output impedance equivalent to that
 of a double cascode.

Analysis, $I_0 = \beta (V_a - V_T)^2$

assume FET Q_1 is saturated (3)

b) $I_0 = (V_{Tm}^2) / R$

assuming $V_T = 25 \text{ mV}$ at 300°K
 then $R = 3.465 \text{ k}\Omega$.

$$T_{CF} = \frac{1}{V_T} \frac{\partial V_T}{\partial T} - \frac{1}{R} \frac{\partial R}{\partial T}$$

$$= \frac{1}{T} - \left(\frac{1}{R} \frac{\partial R}{\partial T} \right)$$

$$= \left(\frac{1}{300} \right) - 1500 \times 10^{-6}$$

$$= \underline{\underline{1.833 \text{ ppm}/^\circ\text{C}}}$$

(4)

Question 4 - continued.

Route of $(Q_3 \rightarrow Q_1)$ cascade

$$R_{out} = (g_{m3} r_{o3} r_{o1})$$

with regulated gate of Q_3

$$R_{out} = (g_{m3} r_{o3} r_{o1}) g_{m2} r_{o2}$$

\Rightarrow assuming $I_B(r_o) \approx \infty$

$$\text{if } \left. \begin{array}{l} g_{m3} = g_{m2} = g_m \\ r_o = r_{o3} = r_{o1} = r_{o2} \end{array} \right\} \rightarrow R_{out} = \underline{\underline{g_m^2 r_o^3}} \quad (5)$$

if gate Q_3 set to a d.c level
then ~~know~~ local feedback to regulate
gate. Node x will swing with
output current and so I_o will change.

Regulating gate of Q_3 ensures that
 $V_{node}(x)$ is reduced by local loop

$$\text{gain } A_2 \approx \underline{\underline{g_{m2} r_{o2}}}$$

(3)

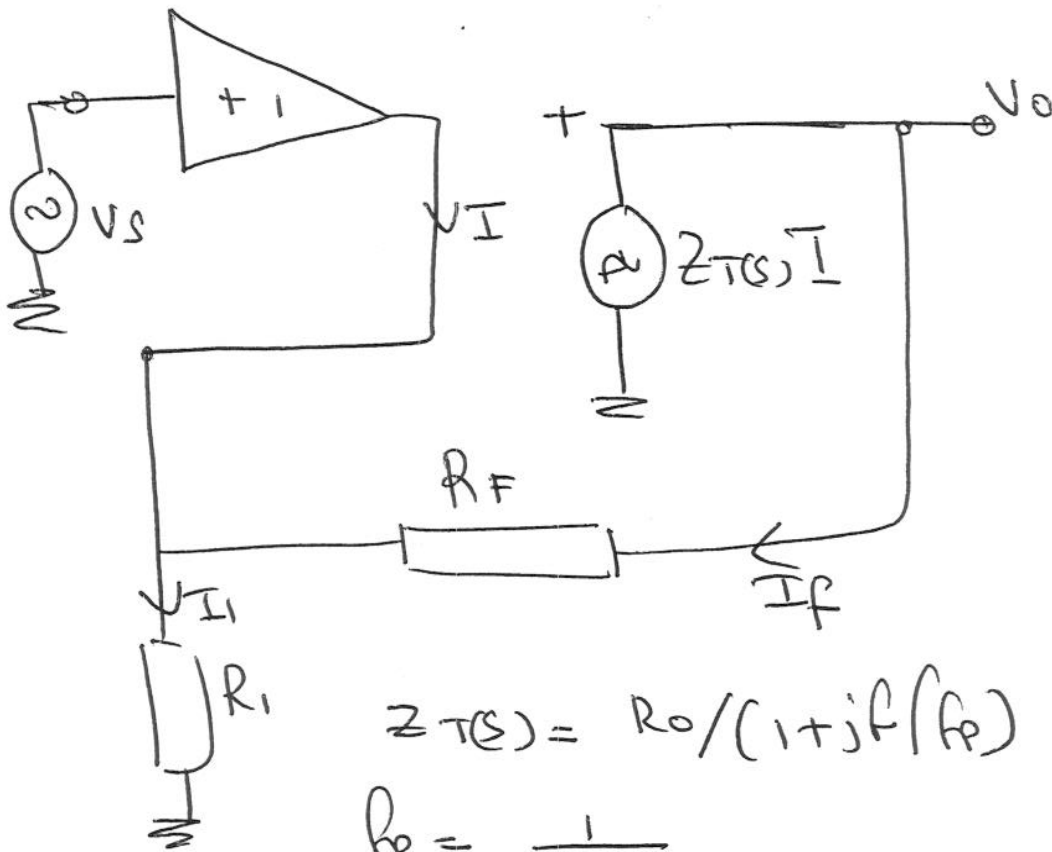
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Advantages of Current-mode

High frequency performance, wide dynamic range

low power supply voltages

4



$$Z_T(s) = R_0 / (1 + jf/f_p)$$

$$f_p = \frac{1}{2\pi R_0 C}$$

C = compensation capacitor

3 equations

$$I_f = (V_o - V_s) / R_f \quad \text{--- (1)}$$

$$I_1 = V_s / R_1 \quad \text{--- (2)}$$

$$V_o = Z_T(s) I = Z_T(s) [I_1 - I_f] \quad \text{--- (3)}$$

8

11

11

Subs (1) and (2) into (3) gives,

$$(V_o/V_s) = (1 + R_F/R_i) Z_T(s) / (R_F + Z_T(s))$$

Subs for $Z_T(s)$ gain

$$(V_o/V_s)_{j\omega} = (1 + R_F/R_i) \left[\frac{R_o}{R_o + R_F} \right] \times \frac{1}{\left(1 + jf / \underbrace{f_p \left[\frac{R_o + R_F}{R_F} \right]}_{\text{BW}} \right)}$$

Assuming $R_o \gg R_F$ BW

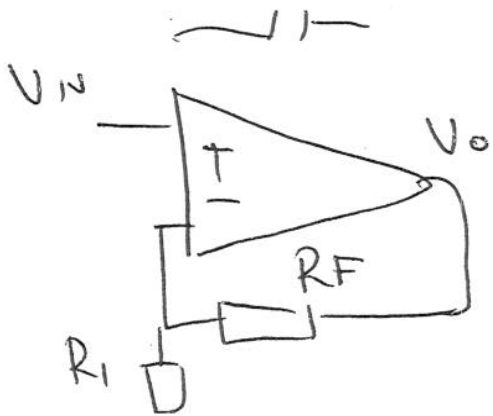
then

Closed loop gain $\approx (1 + R_F/R_i) - *$

Closed loop Bandwidth $\approx \frac{f_p R_o}{R_F} = \frac{1}{2\pi R_F C}$

Hence R_F sets the amplifier constant BW Lx.

and R_i chosen to set the gain



$$BW = \frac{1}{2\pi R_F C} = 10 \text{ MHz}$$

\therefore given $C = 4 \text{ pF}$

$$R_F = 3.98 \text{ k}\Omega$$

Since $A = (1 + R_F/R_i) = 100$

$\therefore R_i = 40.5 \text{ k}\Omega$

Question 6 - Cont

b) Suse stage

Advantage :- High speed
Good phase margin

Disadvantage :- lower gain
lower CMRR/output swing.

(3)

OP-AMP 3(b)

$$\text{Voltage gain} = -g_{m2} / (g_{o2} + g_{o4})$$

$$(g_{o2} + g_{o4}) = I_{D2} (t_n + t_p) =$$

$$5 \times 10^{-6} \times 0.05 = 2.5 \times 10^{-7} \text{ s}$$

$$g_{m2} = 2 \sqrt{\beta_2 I_{D2}} \Rightarrow \beta_2 = \frac{k_p}{2} \left(\frac{W}{L}\right)_2 = 7.5 \times 10^5$$

$$g_{m2} = 3.87 \times 10^{-5} \text{ S}$$

$$A_1 = \underline{\underline{-154.9}}$$

$$(g_{o7} + g_{o6}) = I_{D6} (t_n + t_p)$$

$$= 20 \times 10^{-6} \times 0.05$$

$$= 10 \times 10^{-7} \text{ A/V}$$

$$g_{m6} = 2 \sqrt{\beta_6 I_{D6}} \Rightarrow \beta_6 = \frac{k_p}{2} \left(\frac{W}{L}\right)_6$$

$$= 1.6 \times 10^{-4} \text{ A/V}$$

CT

Question 6(b) continued.

15
15

$$\Rightarrow \omega_m = 1.13 \times 10^{-4}$$

$$A_2 = -113$$

(7)

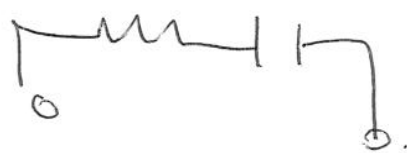
$$A_{\text{total}} = A_1 A_2 = 17503$$

$$Q \cdot B_p = \frac{\omega_m}{2\pi C} = 4.1 \text{ MHz} \quad (2)$$

71-

last part.

Introduce R



improved
phase margin

Feedforward compensation eliminates
RHP zero.

$$\text{Zero given by } z = -\omega_m / C$$

$$\text{with } R \Rightarrow z = -(\omega_m C + R)$$

(3)

GT